REMARKS

Claims 1-21 are pending. Claims 1, 4, 7, 8, 12, 16, and 19 have been amended. Support for the amendments made to claims 1, 4, 7, 8, 12, 16, and 19 may be found, *inter alia*, at pp. 2, 3, and 8-12 of the specification, as well as Figures 3A, 3B, and 4, of the application as filed. No new matter has been added. Reexamination and reconsideration of the present application are respectfully requested.

In the Office Action dated June 6, 2005 (hereinafter referred to simply as the "Office Action"), the Examiner rejected: (1) Claims 1, 4, 12, 13, and 19 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,339,311 to Turner (hereinafter referred to as "Turner"); (2) Claims 1-7, 10-12, and 14-21 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,248,945 to Sasaki (hereinafter referred to as "Sasaki"); and (3) Claims 8-9 and 13 under 35 U.S.C. § 103(a) as being unpatentable over Sasaki in view of Turner. These rejections are respectfully traversed with respect to the claims as amended herein.

The present invention is directed to a system (and corresponding method, computer-readable medium, etc.) for providing packet communications between a server and a client by way of a network, such as, e.g., the Internet. The server inputs data, such as MIDI data, in a sporadic manner, while storing timing data representing the respective input timing of each piece of input data. The server then packetizes the sporadically input data, which accompany the timing data and are transmitted to the client.

The client, in turn, receives the packetized input data and then outputs them, as output data, at timings based on the input timing data, such that the time interval between two consecutive pieces of output data is the same as the time interval between the two consecutive

pieces of (sporadically) input data corresponding to the two pieces of output data. In this way, the time relationship of data during transmission and reception of the sporadically input data is preserved. That is, the original time information representing respective time intervals of (input) data is reproduced upon outputting of the data.

In embodiments of the invention, the timing data (or information) is represented by a series of bits. Thus, in one embodiment, shown generally in Figures 3A and 3B of the instant application as filed, timing data is expressed by an 8-bit shift register, wherein the designation of a "1" in a specific bit position indicates the specific timing at which a piece of data has been input. Similarly, a "0" in a specific bit position indicates that no data has been input (and, therefore, that no data is stored in the buffer register of the RAM 24).

Thus, in the example shown in Figure 3A, e.g., packet timings tn-1, tn, tn+1, tn+2, and tn+3 consecutively occur on the time axis. The server 3 inputs data D1 and D2 during a packet timing interval between the packet timings tn-1 and tn, during which digits "1" and "0" are accumulated in eight bits of timing data Dtn. The input data D1 and D2 (e.g., MIDI data) accompanying the timing data Dtn are collectively transmitted at the packet timing tn. As shown, the timing data Dtn reads "00010010", which indicates that the data D1 is input at a timing corresponding to the fourth bit counted from the leftmost bit, and the data D2 is input at a timing corresponding to the seventh bit.

Where no data is input to the server 3 at all in the period between the packet timing tn and the packet timing tn+1, eight bits of timing data are all set to zero. At the packet timing tn+1, the timing data whose binary notation is "00000000" are stored in the timing data register.

At this time, the buffer register of the RAM 24 stores no data to be transmitted from the server 3 to the client 9.

During the next packet timing interval between packet timings tn+1 and tn+2, the server 3 inputs data D3 and D4, which are stored in the buffer register of the RAM 24 so that the timing data register stores corresponding timing data Dtn+2. The input data D3 and D4 accompanying the timing data Dtn+2 are collectively transmitted at the packet timing tn+2. Thus, the timing data Dtn+2 reads "01000100", which indicates that the data D3 is input at a timing corresponding to the second bit counted from the leftmost bit, and the data D4 is input at a timing corresponding to the sixth bit.

In this way, the server 3 proceeds to collectively transmit the packet corresponding to the combination of the data D1 and D2 accompanying the timing data Dtn at the packet timing tn, followed by collective transmission of the packet corresponding to the combination of the data D3 and D4 accompanying the timing data Dtn+2 at the packet timing tn+2. Thus, the server 3 packetizes the input data (e.g., MIDI data) and timing data at each packet timing and transmits the packetized data to the client 9 over a network 40.

The client 9, in turn, receives the packetized data consisting of the input data and timing data by means of a communication interface 31, and proceeds to separate the input data and timing data. That is, the timing data are stored in the timing data register of the RAM 24, while the received data (i.e., received MIDI data) are stored in the buffer register of the RAM 24. When a "1" is output from the timing data register, the client 9 reads and outputs one data from the buffer register of the RAM 24. Therefore, each of the received data is to be output from the client 9 in accordance with a corresponding "1" from the timing data register. In this way, the

client 9 outputs each piece of received data (to a sound source 10) in complete synchronization with the prescribed timing that substantially corresponds to the timing at which the sever 3 inputs each data by the packet timing.

Using the example of Figure 3A, and with reference to Figure 3B, as noted above, the server 3 inputs the data D1 at the fourth shift timing counted from the packet timing tn-1; then, it inputs the data D2 at the seventh shift timing. These pieces of data D1 and D2 are transmitted to the client 9, wherein they are stored in the RAM 24 in connection with the timing data Dtn. Thereafter, the client 9 outputs the data D1 at the fourth shift timing that is counted from the prescribed packet timing substantially matching the packet timing tn-1. Then, the client outputs the data D2 at the seventh shift timing.

Similarly, the server 3 inputs the data D3 at the second shift timing counted from the packet timing tn+1; then, it inputs the data D4 at the sixth shift timing. These pieces of data D3 and D4 are transmitted to the client 9, wherein they are stored in the RAM 24 in connection with the timing data Dtn+2. Thereafter, the client 9 outputs the data D3 at the second shift timing that is counted from the prescribed packet timing substantially matching the packet timing tn+1. Then, the client outputs the data D4 at the sixth shift timing. Therefore, an original time interval between the input data D1 and D2, as well as D3 and D4, respectively, input to the server 3 is completely preserved in the client 9, which outputs the data D1 and D2, as well as D3 and D4, respectively, to the sound source 10.

Claim 1, as amended herein, recites (emphasis added):

> 1. A communication method that is executed by a transmission unit and a reception unit, comprising:

> packetizing sporadically input data to accompany timing information representing respective input timings of the input data, said timing information being represented by a series of bits, wherein, within a given time interval, a bit value of "1" indicates an input timing for a specific piece of input data;
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> transmitting packetized input data accompanying the timing information from the transmission unit;
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> receiving the packetized input data accompanying the timing information by the reception unit; and
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> outputting the packetized input data as output data at timings based on the timing information from the reception unit, wherein consecutive pieces of said output data are outputted at the same relative timings as the relative input timings of the corresponding input data.

As an initial matter, it is respectfully submitted that the limitation of the timing information, or data, "being represented by a series of bits, wherein, within a given time interval, a bit value of "1" indicates an input timing for a specific piece of input data" is not disclosed or taught by Turner and/or Sasaki.

In rejecting claim 8, which, as examined, contained a reference to "a packet timing that occurs by a prescribed number of shift timings corresponding to bits of the timing data" and, as such, bore the closest relationship to the above-mentioned limitation in amended claim 1, the Examiner states that (*see* Office Action, p. 8; emphases added):

> In regards to claim 8, Sasaki discloses the transmission unit according to claim 7, Sasaki does not discloses [sic] wherein the prescribed time corresponds to a packet timing that occurs by a prescribed number of shift timings corresponding to bits of the timing data respectively, so that the input timings are represented by the bits of the timing data.
>
> Turner discloses wherein the prescribed time corresponds to a packet timing that occurs by a prescribed number of shift timings corresponding to bits of the timing data respectively, so that the input timings are represented by the bits of the timing data (col. 4, ll. 12-col. 5, ll. 4).

> It would be obvious to one of ordinary skill in the art at the time of the invention to modify Sasaki by having packet timing that occurs by a prescribed number of shift timings corresponding to bits, as taught by Turner in order to determine the sequence in which packets thereby [sic] by controlling the transmission of data packets (col. 2, ll. 11-47).

However, it is respectfully submitted that col. 4, line 12 – col. 5, line 4 of Turner do not disclose bit information that represents the input timings of the input data. More specifically, the cited section of Turner references a bi-directional shift register (BSR) 60, which "contains the number of the buffer slot managed by this control slot at its left end and the age for the stored data packet with the age's most significant bit at the right end of the shift register." *See* Turner, col. 4, lines 46-50. The "age", in turn, is defined as follows (col. 3, lines 59 – 65; emphasis added):

> Incoming data packets have a time stamp representative of their time of entry into the switch 22 which is compared with the current time to generate an age, the age then being stored along with an associated slot number, the slot number being that position in the resequencing buffer 44 where the data packet is stored.

Thus, although Turner discloses storage of information (i.e., the age of the data packet) that is derived from the data packet's input timing, there is no disclosure or teaching of storing the input timing of each data packet itself, much less of storing the input timing by bit representation. In addition, Turner does not disclose, or even suggest, a bit-based structure for registering time information only (as opposed to both age and slot number information), let alone one in which a "1" in a given bit position represents the input timing for a specific piece of input data, and a "0" represents the absence of input data at that point.

In addition, as conceded by the Examiner, Sasaki discloses nothing at all in connection with the representation of timing information for input data by a series of bits. As such, it is respectfully submitted that Tuner and Sasaki do not disclose, suggest, or teach, either

individually or in combination, the limitation in amended claim 1, of *timing information being represented by a series of bits, wherein, within a given time interval, a bit value of "1" indicates an input timing for a specific piece of input data.*

The above-noted shortcoming of Turner makes sense, of course, given the problem that is being addressed by Turner. That is, as has been noted by the Examiner (see above-noted excerpt from the Office Action, p. 8), Turner, by its very own terms, is limited to reproducing the correct sequence, and not the relative timing, of a series (or consecutive pieces) of input data. Thus, for example, Turner provides that (*see* col. 1, lines 48 – 62):

> The resequencer of the present invention includes a resequencer buffer which receives the data packets after they exit from the switch, and its associated buffer controller which controls the buffer to output the data packets in time sequence as opposed to the strict sequence in which they are received from the switch. Additionally, a time stamp circuit at the input side of the switch stamps the data packets with the current time as they enter the switch. Therefore, as the data packets exit the switch, they contain a time stamp representative of their sequence as they entered the switch. As the data packet exits the switch and enters the resequencing buffer, its time stamp is compared with the then current time to generate a delta T which is equivalent to the time lapse for that particular packet to traverse the switch.

That is, the problem to be solved, and Turner's solution to that problem, involve correct sequencing, or ordering, of the data packets at the output side, and not reproduction, or output, of data at the same time intervals as those for the corresponding input data. As noted previously, it is for this reason that, for the purposes of the invention disclosed in Turner, storage merely of the age, as opposed to the actual timing, of the input data will suffice.

It is therefore respectfully submitted that Tuner and Sasaki do not disclose, suggest, or teach, either individually or in combination, the additional limitation in amended claim 1, of *outputting the packetized input data as output data at timings based on the timing information*

from the reception unit, wherein consecutive pieces of said output data are outputted at the same relative timings as the relative input timings of the corresponding input data. In light of the above, the Applicants respectfully submit that claim 1, as amended, distinguishes over the cited art and is in condition for allowance. As such, it is respectfully requested that the rejection of claim 1 be withdrawn.

Each of independent claims 4, 7, 12, 16, and 19 has also been amended herein to include limitations similar to those discussed above in connection with claim 1. As such, and in light of the above discussion, it is respectfully submitted that claims 4, 7, 12, 16, and 19 distinguish over the cited references for at least the same reasons as those noted above in connection with amended claim 1. The Applicants therefore respectfully request that the rejections as to claims 4, 7, 12, 16, and 19 be withdrawn, as these claims are now believed to be in condition for allowance.

In addition, claims 2-3 depend directly from claim 1, claims 5-6 depend directly from claim 4, claims 8-11 depend directly from claim 7, claims 13-15 depend directly from claim 12, claims 17-18 depend directly from claim 16, and claims 20-21 depend directly from claim 19. As such, it is respectfully submitted that claims 2-3, 5-6, 8-11, 13-15, 17-18, and 20-21 also distinguish over the cited art for at least the same reasons as those noted above in connection with amended claim 1. Therefore, the Applicants respectfully request that the rejection of claims 2-3, 5-6, 8-11, 13-15, 17-18, and 20-21 be withdrawn, as these claims are also believed to be in condition for allowance.

It is believed that claims 1-21, as amended herein, are in condition for allowance, and a favorable action is respectfully requested. If, for any reason, the Examiner finds the application

other than in condition for allowance, the Examiner is requested to call one of the undersigned attorneys at the Los Angeles, California telephone number (213) 488-7100 to discuss the steps necessary for placing the application in condition for allowance.

Respectfully submitted,
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